(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :08/02/2025

(21) Application No.202541010762 A
(43) Publication Date : 14/02/2025

(54) Title of the invention : Novel Interconnect Design for Reducing Signal Crosstalk in VLSI Circuits

(51) International classification :H05K0001020000, H01L0023660000, H01L0021768000, G06F0030367000, G02B0006420000
(86) International Application No :NA
Filing Date :NA
(87) International Publication No : NA
(61) Patent of Addition to Application Number :NA
Filing Date :NA
(62) Divisional to Application Number :NA
Filing Date :NA

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(57) Abstract :
ABSTRACT Novel Interconnect Design for Reducing Signal Crosstalk in VLSI Circuits The invention provides a novel interconnect design for reducing signal crosstalk in Very Large Scale Integration (VLSI) circuits. As transistor densities increase in modern semiconductor technologies, the proximity of adjacent signal lines leads to increased electromagnetic interference, which causes crosstalk. This crosstalk results in signal degradation, noise, and timing errors, adversely affecting the performance and reliability of high-speed circuits. The present design incorporates advanced strategies such as staggered signal line arrangements, strategically placed grounding shields, and the use of low-k dielectric materials to effectively mitigate crosstalk, ensuring improved signal integrity. The interconnect design enhances the overall performance of VLSI circuits by addressing the critical issue of signal interference without requiring excessive chip area. By optimizing the spacing between signal lines based on their importance and strategically integrating shielding, the invention reduces unwanted signal coupling while maintaining efficient use of the available chip space. The incorporation of low-k dielectric materials lowers capacitance between adjacent signal lines, further reducing the potential for crosstalk and improving the power efficiency of the circuit. This invention is particularly relevant for future generations of VLSI technologies, where process nodes are expected to shrink even further, making crosstalk a more significant challenge. The proposed interconnect design is scalable and adaptable to smaller nodes such as 5 nm and beyond, ensuring that it remains effective as technology evolves. Additionally, the design improves manufacturing efficiency by minimizing the need for complex fabrication processes, reduces power consumption, and optimizes circuit performance, making it an ideal solution for next-generation semiconductor devices.

No. of Pages : 16 No. of Claims : 5