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(57) Abstract :
ABSTRACT A Power-Optimized VLSI Framework for Edge AI Inference in IoT-Based Smart Devices The invention discloses a power-optimized Very Large-Scale Integration (VLSI) framework specifically designed to enhance the efficiency of edge Artificial Intelligence (AI) inference in Internet of Things (IoT)-based smart devices. As IoT ecosystems grow increasingly complex, the demand for energy-efficient and real-time AI processing at the edge has become critical. Traditional cloud-based AI inference suffers from latency, high bandwidth usage, and power consumption constraints, creating a need for a dedicated on-chip hardware framework optimized for low-power operations. The proposed framework integrates specialized hardware accelerators, dynamic voltage and frequency scaling (DVFS), memory-efficient architectures, and approximate computing strategies to minimize power consumption while maintaining high accuracy and performance. It incorporates parallelized processing units and hierarchical memory management to support deep learning workloads with reduced computational overhead. This ensures that edge devices can perform AI inference tasks such as image recognition, anomaly detection, and predictive analytics without relying on high-power external resources. By combining architectural optimization with intelligent power management techniques, the framework provides a scalable and sustainable solution for next-generation IoT deployments. The invention is particularly beneficial in applications such as smart healthcare monitoring, autonomous vehicles, industrial automation, and environmental sensing, where continuous real-time AI inference is required under strict power constraints. The disclosed framework therefore establishes a foundation for low-power, high-performance AI-driven IoT devices that can operate reliably in energy-limited environments.

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